Direct Parameter Extraction on RF-CMOS

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Abstract — **The good knowledge of all parameters of the models used with the circuit simulations is one of the major prerequisites for a successful design. This is particularly true for the design of analog radio-frequency (RF) circuits. An efficient and accurate method to directly extract the parameters needed for accurate modeling of transistors in a standard CMOS sub-micron technology for RF-applications is presented. The paper concentrates on the extraction procedure, with emphasis on its simplicity, hence excluding fitting or optimization, and on the accuracy of its results. The extracted parameters are applied to a first order non-quasistatic (NQS) model and the simulation results compared with measurements. Excellent agreement between simulations and measurements up to 50GHz is achieved.**

I. Introduction

The subject of parameter extraction on active integrated devices for high frequency applications has been dealt with quite frequently over the last several years [1-7]. The strategies for parameter extraction on CMOS technologies use full [5,7] or partial [3,6] parameter fitting, presuppose knowledge of some parameters [1] or assume device symmetry [6].

The present work uses the previous work of Lee et al [3] and Raskin et al [4], but provides an improvement on two crucial points:

1) Neither [3] nor [4] do account for the effect of the substrate resistance. While the latter is absent in SOI-technologies [4], neglecting the substrate network in bulk CMOS might lead to large simulation errors. In this work the effect of the substrate is accounted for and a method for the direct extraction of the corresponding parameters is presented.
2) [3] and [4] use curve fitting at least to some extend to obtain certain parameter values. The present work describes how to obtain, through direct extraction, a unique value for each parameter, which can be included in the model without further fitting or tuning.

The paper is organized as follows: Section II shortly presents the small signal model used in this work and its possible simplifications under certain bias conditions, section III describes the extraction procedure, section IV presents the validation of the extraction methodology on a standard 0.18µm CMOS technology and section V adds some concluding remarks.

II. Small Signal Models

A first-order non-quasistatic (NQS) model [8] including the extrinsic elements (access impedances, overlap capacitances and diffusion capacitances) is shown in fig. 1.

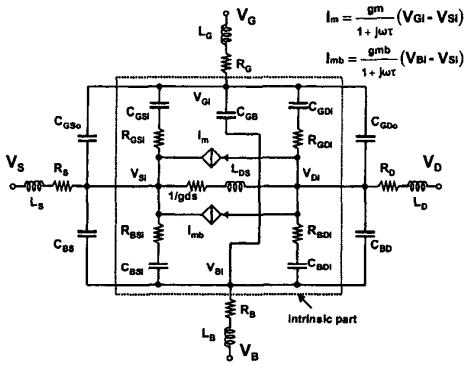

Fig. 1. The first order non-quasistatic MOS-model [8].

It is obvious that, due to complexity of this model, a direct extraction of all its parameters is impossible. Global fitting of the full model to measurements, however, will tend to produce unphysical parameter values.

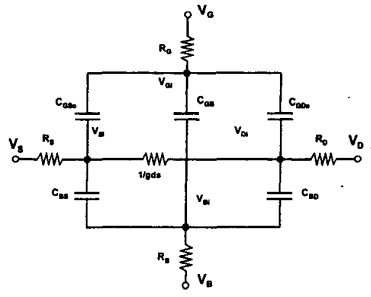

Fig. 2. A model for the MOS transistor in accumulation or depletion.

By exploiting the different operating regions of the MOS transistor, various levels of simplification can be

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applied to the model of fig.1. Fig. 2 shows the equivalent circuit of a MOS-transistor biased from accumulation to depletion with V_{DS}=0V. Due to the high impedance environment, the inductances L_s, L_d, L_g, and L_b can be neglected under these bias conditions (a 100pH inductance represents about 300Ω at 50GHz). The MOS-transistor, biased in the triode region (V_{DS}=0V) from weak to strong inversion, is described by the model of fig. 1 with I_m=I_{mb}=0.

III. The Extraction Procedure

The inner nodes of the circuit in fig.2 are considered as a 3-port with inner bulk node V_{bi} grounded. The Y-parameter matrix is obtained by solving the current equations in (1) with V_{bi}=0 and by respectively setting pairs of the other node voltages to zero.

$$\begin{aligned} I_g &= s\cdot C_{gb}\cdot(V_{gi}-V_{bi}) + s\cdot C_{gs}\cdot(V_{gi}-V_{si}) + s\cdot C_{gd}\cdot(V_{gi}-V_{di}) \\ I_d &= gds\cdot(V_{di}-V_{si}) + s\cdot C_{gd}\cdot(V_{di}-V_{gi}) + s\cdot C_{bd}\cdot(V_{di}-V_{bi}) \\ I_s &= gds\cdot(V_{si}-V_{di}) + s\cdot C_{gs}\cdot(V_{si}-V_{gi}) + s\cdot C_{bs}\cdot(V_{si}-V_{bi}) \end{aligned} \quad (1)$$

The 3-port Y-parameter matrix is then transformed into the corresponding Z-parameter matrix and the access resistances are added (2)[3,4]:

$$\underline{\underline{Z}}_{tot} = \underline{\underline{Z}}_0 + \underline{\underline{R}} + \underline{\underline{R}}_B$$
$$\underline{\underline{R}} = \begin{pmatrix} R_g & 0 & 0 \\ 0 & R_d & 0 \\ 0 & 0 & R_s \end{pmatrix} \text{ and } \underline{\underline{R}}_B = \begin{pmatrix} R_b & R_b & R_b \\ R_b & R_b & R_b \\ R_b & R_b & R_b \end{pmatrix} \quad (2)$$

The 3-port impedance matrix is then reduced to a 2-port Z-matrix by grounding the external source node V_s.

A. Extraction of the access resistances

Further analysis of the Z-parameters shows that, at the limit of infinite frequency, the real parts of the 2-port Z-matrix approach the following values:

$$R\{Z_{11}\}\big|_{f\to\infty} = R_g + R_s // R_b \;;\; R\{Z_{12}\}\big|_{f\to\infty} = R_s // R_b \;;$$
$$R\{Z_{22}\}\big|_{f\to\infty} = R_d + R_s // R_b \;; \quad (3)$$

They exhibit the same dependence on frequency, hence a straight line is obtained by plotting one against the other on a parametric plot [4] (see fig.3). This behavior can only be observed as long as the transistor is not biased in its active region. In the latter case the parametric plot shows a change in slope at relatively high frequencies due to the substrate network.

By means of linear regression of the parametric plots $R\{Z_{11}\}$ versus $R\{Z_{12}\}$ and $R\{Z_{22}\}$ versus $R\{Z_{12}\}$, respectively, the values of R_g and R_d can be expressed as functions of R_s//R_b (4):

$$\begin{aligned} R_g &= IC_{11} + (1-k_{11})\cdot R_s // R_b \\ R_d &= IC_{22} + (1-k_{22})\cdot R_s // R_b \end{aligned} \quad (4)$$

where IC and k are the intercept and slope of the respective linear regressions.

Under these bias conditions and at sufficiently high frequencies the parametric plot of $R\{Z_{12}\}$ versus $I\{Z_{12}\}/\omega$ becomes linear (fig.4) and $I\{Z_{12}\}/\omega$ tends towards zero at infinite frequency. Hence, the intercept with the Y-axis of the tangent on the high frequency end of this parametric plot equals R_s//R_b.

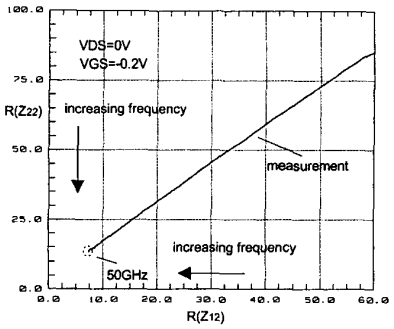

Fig. 3. Parametric plot of $R\{Z_{22}\}$ versus $R\{Z_{12}\}$.

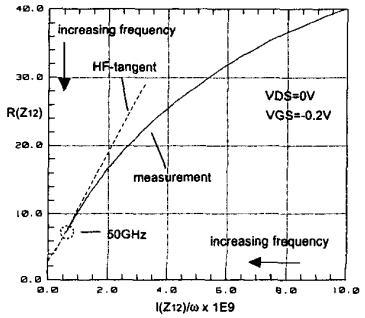

Fig. 4. Parametric plot of $R\{Z_{12}\}$ versus $I\{Z_{12}\}/\omega$.

It is important to note that the extraction does not presuppose the symmetry between source and drain, which could lead to errors in the extracted parameter values.

B. Extraction of the substrate resistance

Different levels of sophistication of the substrate-network have been proposed in literature [7]. A direct extraction procedure requires the reduction of this network to a single lumped resistor R_b as shown in fig.2. As long as the channel is in accumulation or depletion, a pronounced

signature of R_b can be found in the plot of the real part of Z_{12} versus frequency, which shows a 40dB drop in magnitude due to the presence of a double-pole. The magnitude of $R\{Z_{12}\}$ is 6dB below the plateau for the very frequency, at which the 4th order and the 6th order component of the denominator become equal. This relation is shown in (5) whereas (6) presents the relation used to calculate R_b from the extracted frequency.

$$[C_{gd}\cdot(C_{gb}+C_{gd})+C_{bd}\cdot(C_{gb}+2C_{gd})]^2 = [(C_{bd}+C_{gd})[C_{gb}\cdot C_{gd}+C_{bd}\cdot(C_{gb}+2C_{gd})](R_b+Rs)\omega_{-6dB}]^2 \quad (5)$$

$$R_b = \frac{1}{\omega_{-6dB}\cdot(C_{gd}+C_{bd})}\cdot\left[1+\frac{1}{2\cdot(1/C_{gd}+1/C_{bd})}\right]-Rs \quad (6)$$

Fig. 5 presents the measured $R\{Z_{12}\}$ in decibel versus frequency, the level from which the 6dB drop in magnitude is calculated and the double-pole function derived from (6) above.

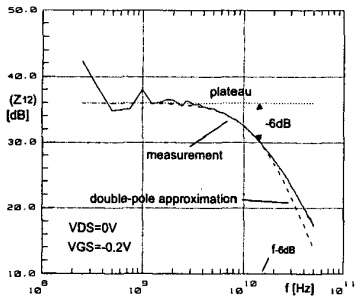

Fig. 5. Extraction of R_b on $R\{Z_{12}\}$

Due to the shift to higher frequencies of a low frequency pole, which is linked to the output conductance gds, the pronounced plateau (i.e. the reference level for the extraction of R_b) disappears at the onset of weak inversion.

C. Extraction of capacitances and inductances

The Y-parameters measured on devices biased with V_{DS}=0V and below threshold allow the extraction at low frequencies of the gate-drain overlap capacitance through $C_{gdo}=|I\{Y_{12}\}|/\omega$, the drain-bulk diffusion capacitance through $C_{bd}=I\{Y_{22}\}/\omega$ - C_{gdo} and the gate-bulk accumulation or depletion capacitance through $C_{gb}=I\{Y_{11}\}/\omega$ - (C_{gso} + C_{gdo}). C_{gso} and C_{bs} cannot be obtained directly from 2-port measurements. Their values, however, differ in general only slightly from the values obtained for C_{gdo} and C_{bd} respectively due to the multi-finger layout generally used for MOS-devices in RF-applications. The above relation for the extraction of the drain-bulk diffusion capacitance is also valid at $V_{DS}>0V$ and $V_{GS}<V_{TH}$.

The measurement of the device in the triode region (V_{DS}=0V and $V_{GS}>V_{TH}$) allows determining the intrinsic gate-drain capacitance C_{gdi} and the gate-bulk capacitance C_{gb} at the onset of inversion. In strong inversion and triode region, the relation $C_{gdi}=I\{Y_{11}\}/2\omega-(C_{gso}+C_{gdo}+C_{gbo})$ becomes valid, where C_{gbo} is the gate-bulk overlap capacitance, which is constant with bias and generally small in value. The inductances L_s and L_d are extracted at the high frequency limit of the relations $I\{Z_{12}\}/\omega$ and $I\{Z_{22}\}/\omega$ - L_s respectively (channel in deep strong inversion to make the NQS-equivalent inductance L_{ds} negligible). The gate inductance L_g could be extracted from $I\{Z_{22}\}/\omega$ - L_s, but was too small in our case to be visible even at frequencies as high as 50GHz.

IV. Validation of the Extraction Procedure

RF-transistors and their corresponding deembedding structures (open and short) have been implemented in a 0.18µm CMOS technology and measured under different bias conditions (sign-inversion for P-type transistors):

1) V_{GS} from –1V to 0.2V with V_{DS}=0V
2) V_{GS} from 0.3V to 2.5V with V_{DS}=0V
3) V_{DS} from -0.4V to 2V with V_{GS}=–0.5V
4) V_{GS} from 0V to 1.8V and V_{DS} from 0V to 1.5V

The model in fig. 1 is used for the simulations. For the operation in strong inversion triode region, the parameters $R_{gsi}=R_{gdi}$, $C_{bsi}=C_{bdi}$, $R_{bsi}=R_{bdi}$, L_{ds} are calculated from the extracted C_{gdi}-value according to [8] with η=1 (at V_{DS}=0V) and $\omega_0=\mu(V_{GS}-V_{TH})/(nL_{eff}^2)$.

TABLE I
PARAMETERS EXTRACTED ON DIFFERENT MOS-DEVICES

	Rg	Rs	Rd	Rb	C_{BD}	Ls	Ld
NMOS	Ω	Ω	Ω	Ω	fF	fF	pH
16x4/0.18	3.8	3.1	4.1	191	48	3.5	1.5
16x4/0.25	2.2	4.5	6.1	170	47	3.4	1.7
16x4/0.4	1.1	5.7	6.3	139	46	X	X
16x4/1.0	0.7	9.8	9.9	72	44	X	X
16x8/0.18	3.4	1.6	1.6	162	95	5.0	1.9
24x4/0.18	2.5	2.9	4.8	121	70	5.6	2.5
32x4/0.18	1.7	2.5	3.9	97	94	6.5	3.1
32x2/0.18	1.8	4.3	6.1	102	50	5.1	2.4
PMOS							
16x4/0.18	2.5	4.1	6.2	57	57	X	X

Fig. 6 shows measurements and simulation results on an NMOS with 16 fingers of 4µm width and 0.18µm length (16x4/0.18) for two bias points. Note that the good

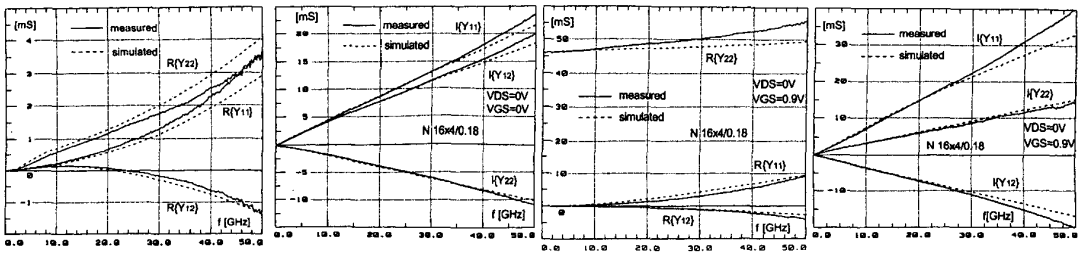

Fig. 6. Comparison for two operating points of measured (solid lines) and simulated (dashed lines) Y-parameters of an NMOS with 16 fingers of 4/0.18μm up to 50GHz.

agreement between measurements and simulations up to very high frequencies is obtained by directly using the extracted parameters without fitting or tuning. In fig. 7 the extracted resistances are shown for the same device versus V_{GS}. The bias dependence of the access resistors R_g, R_s and R_d, which can be observed in fig. 7 towards weak inversion, cannot be discussed within the scope of this paper. Table I lists some parameters for a set of transistors, extracted following the procedure of section III. Good scaling behavior of the devices can be observed.

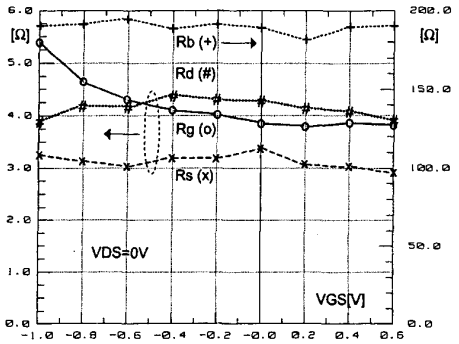

Fig. 7. R_g, R_s, R_d and R_b extracted on an NMOS of 16x4/0.18μm for V_{DS}=0V and V_{GS} between −1.0V and 0.6V

V. Conclusion

An accurate and efficient procedure for the extraction of parameters for the modeling of RF CMOS-transistors has been presented. It has been demonstrated that the method allows the reliable determination of parameters down to very small values. The extraction of the parameters bias dependence and scaling behavior can be used to establish a model, which takes these features into account. This subject, however, is out of the scope of this paper.

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